

N-Channel Power MOSFET

500V, 4A, 2.7Ω

FEATURES

- 100% UIS and R_g tested
- Advanced planar process
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

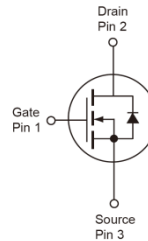
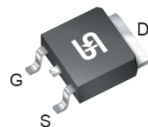
PARAMETER	VALUE	UNIT
V _{DS}	500	V
R _{DS(on)} (max)	2.7	Ω
Q _g	12	nC

APPLICATIONS

- AC/DC LED Lighting
- Power Supply
- Charger



TO-252 (DPAK)



Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	Limit	UNIT
Drain-Source Voltage	V _{DS}	500	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current ^(Note 1)	I _D	T _C = 25°C	4
		T _C = 100°C	2.5
Pulsed Drain Current ^(Note 2)	I _{DM}	16	A
Total Power Dissipation @ T _C = 25°C	P _{DTOT}	83	W
Single Pulse Avalanche Energy ^(Note 3)	E _{AS}	78.4	mJ
Single Pulse Avalanche Current ^(Note 3)	I _{AS}	2.8	A
Operating Junction and Storage Temperature Range	T _J , T _{STG}	- 55 to +150	°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	Limit	UNIT
Junction to Case Thermal Resistance	R _{θJC}	1.5	°C/W
Junction to Ambient Thermal Resistance	R _{θJA}	62	°C/W

Thermal Performance Note: R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. R_{θJA} is guaranteed by design while R_{θCA} is determined by the user's board design. R_{θJA} shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	500	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2	2.2	3	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 4)	$V_{GS} = 10V, I_D = 1.7A$	$R_{DS(on)}$	--	2.4	2.7	Ω
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 400V, I_D = 3.4A,$ $V_{GS} = 10V$	Q_g	--	12	--	nC
Gate-Source Charge		Q_{gs}	--	2.2	--	
Gate-Drain Charge		Q_{gd}	--	4.4	--	
Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	453	--	pF
Output Capacitance		C_{oss}	--	27	--	
Reverse Transfer Capacitance		C_{rss}	--	1	--	
Gate Resistance	$f = 1.0MHz$	R_g	--	2.6	5.2	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 250V, R_G = 5\Omega,$ $I_D = 3.4A, V_{GS} = 10V$	$t_{d(on)}$	--	5.4	--	ns
Turn-On Rise Time		t_r	--	18.4	--	
Turn-Off Delay Time		$t_{d(off)}$	--	12.4	--	
Turn-Off Fall Time		t_f	--	19.6	--	
Source-Drain Diode						
Forward Voltage (Note 4)	$I_S = 3.4A, V_{GS} = 0V$	V_{SD}	--	--	1.3	V
Reverse Recovery Time	$I_S = 3.4A$	t_{rr}	--	233	--	ns
Reverse Recovery Charge	$di_f/dt = 100A/\mu s$	Q_{rr}	--	0.84	--	μC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 20mH, I_{AS} = 2.8A, V_{DD} = 50V, R_G = 25\Omega,$ Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s,$ duty cycle $\leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

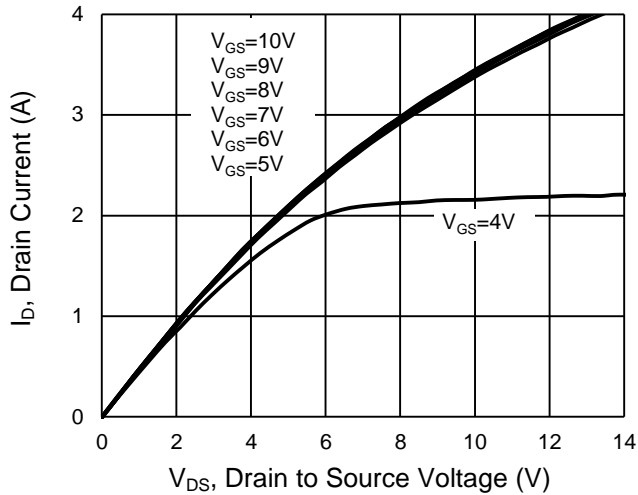
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM4NC50CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

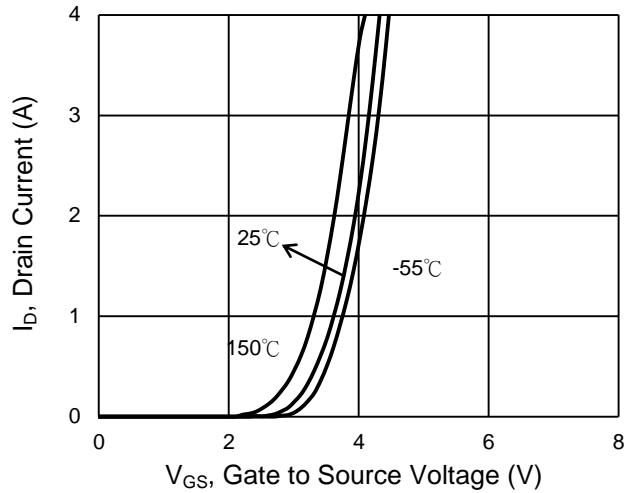
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

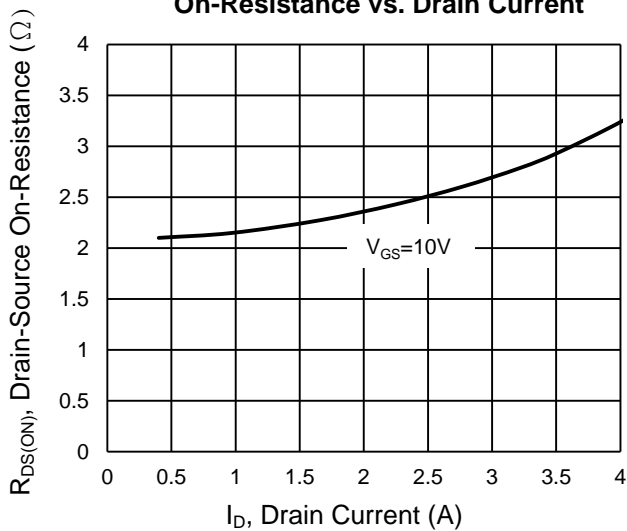
Output Characteristics



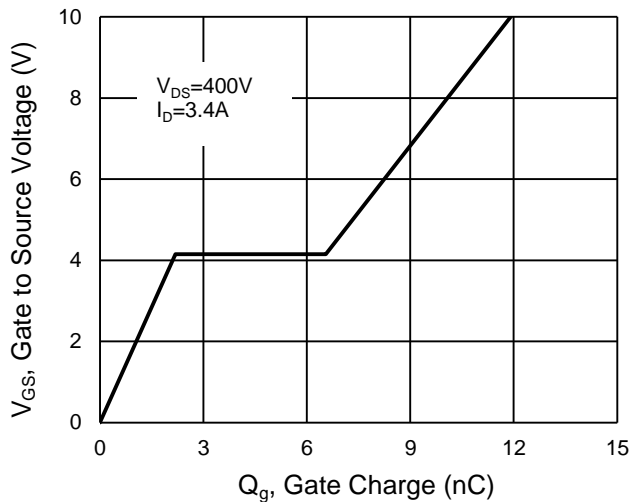
Transfer Characteristics



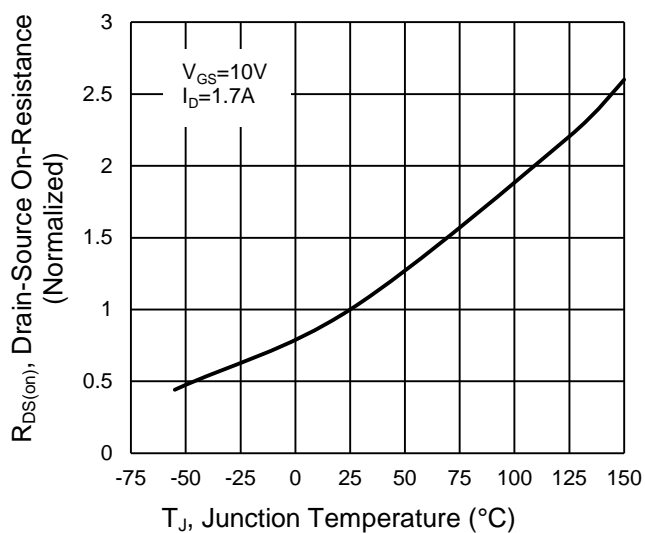
On-Resistance vs. Drain Current



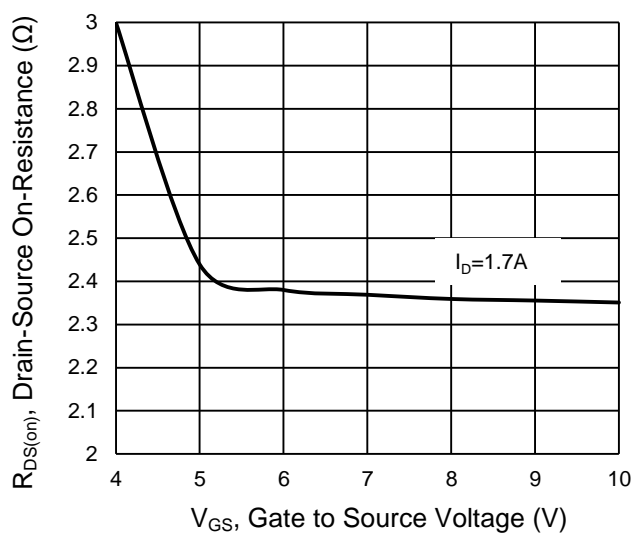
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



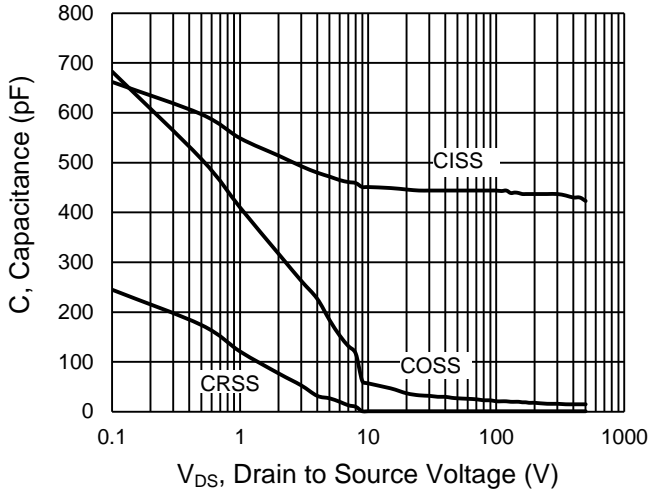
On-Resistance vs. Gate-Source Voltage



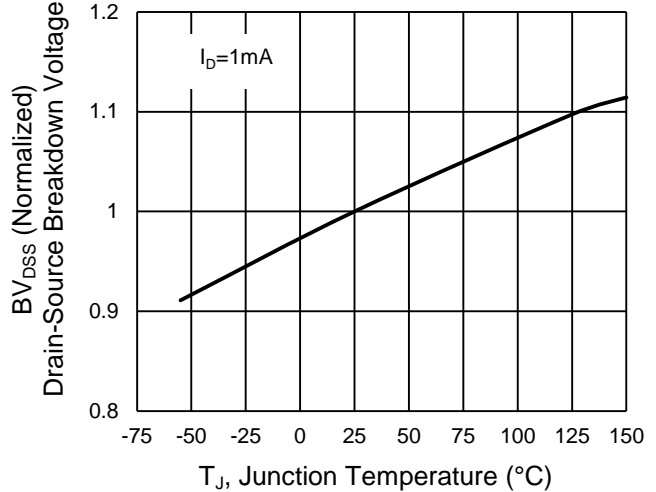
CHARACTERISTICS CURVES

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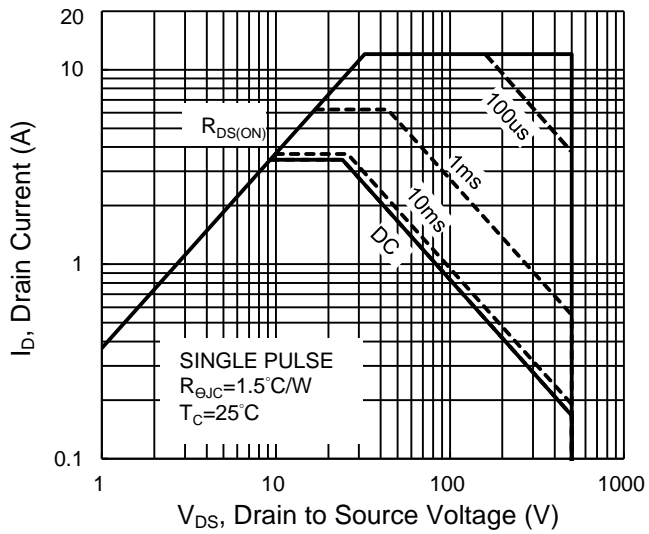
Capacitance vs. Drain-Source Voltage



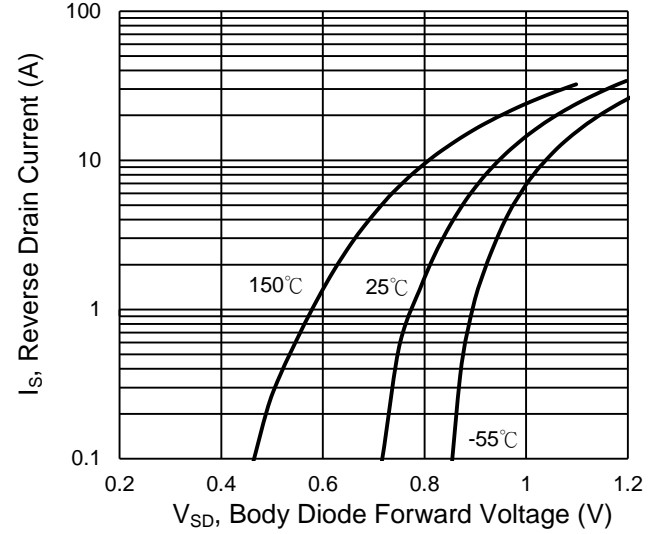
BV_{DSS} vs. Junction Temperature



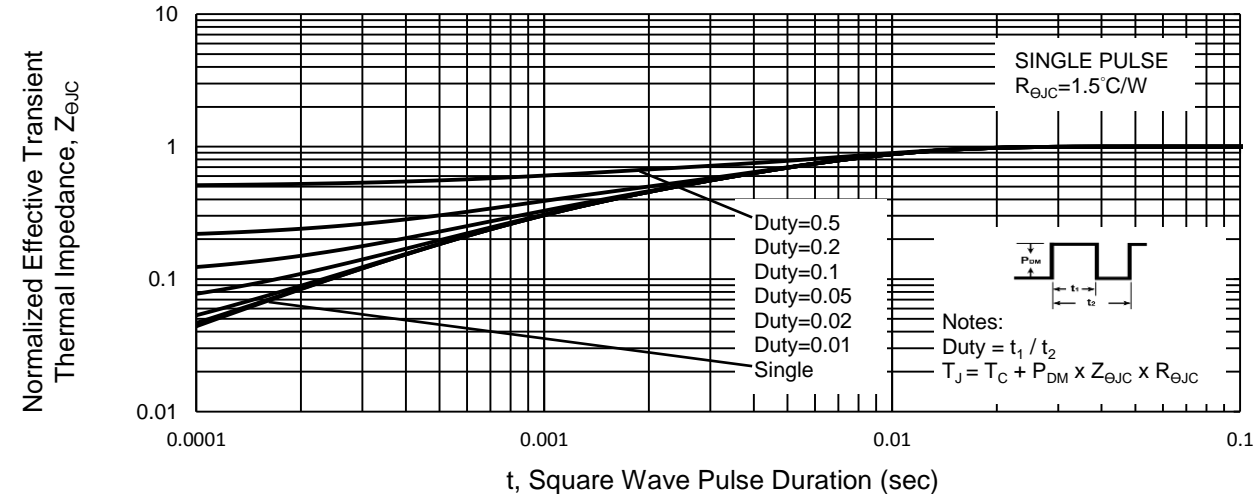
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

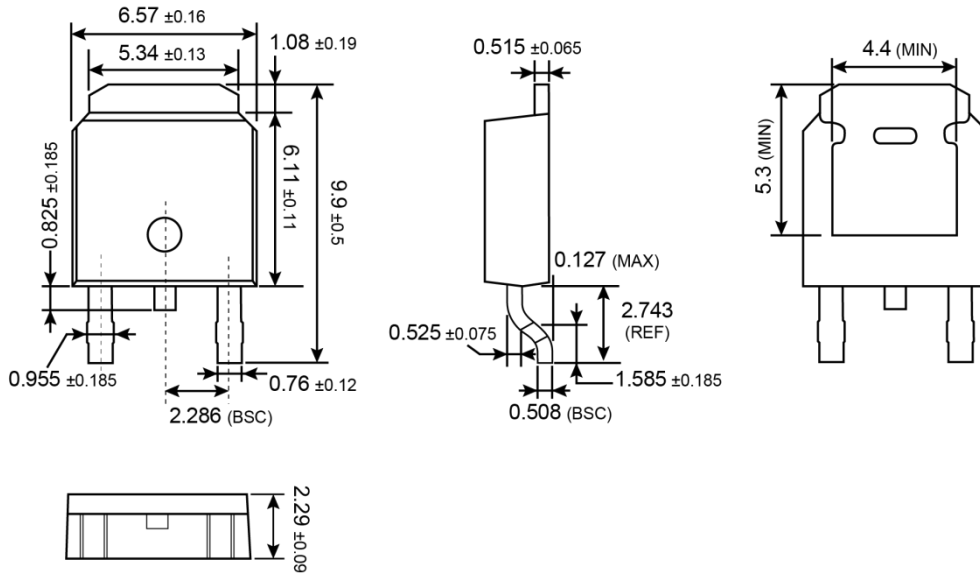


Normalized Thermal Transient Impedance, Junction-to-Case

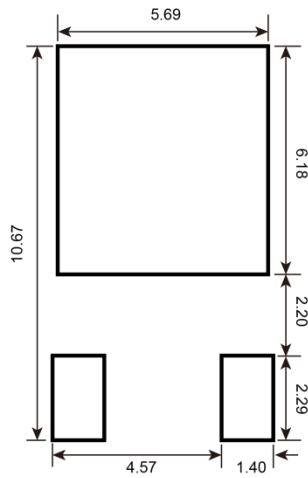


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

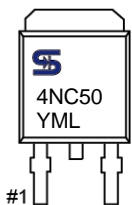
TO-252



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- M** = Month Code
- O** =Jan **P** =Feb **Q** =Mar **R** =Apr
- S** =May **T** =Jun **U** =Jul **V** =Aug
- W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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