SLG7NT4192

GreenPAK 3™

Power Good Generator Logic

General Description

Silego SLG7NT4192 is a low power and small form device. The SoC is housed in a 2mm x 3mm TQFN package which is optimal for using with small devices.

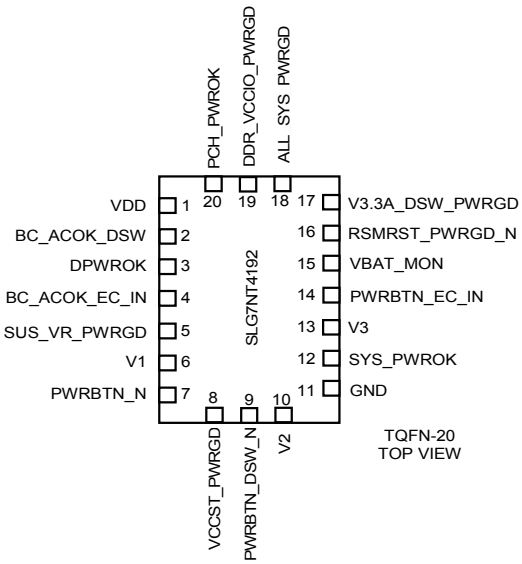
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- TQFN-20 Package

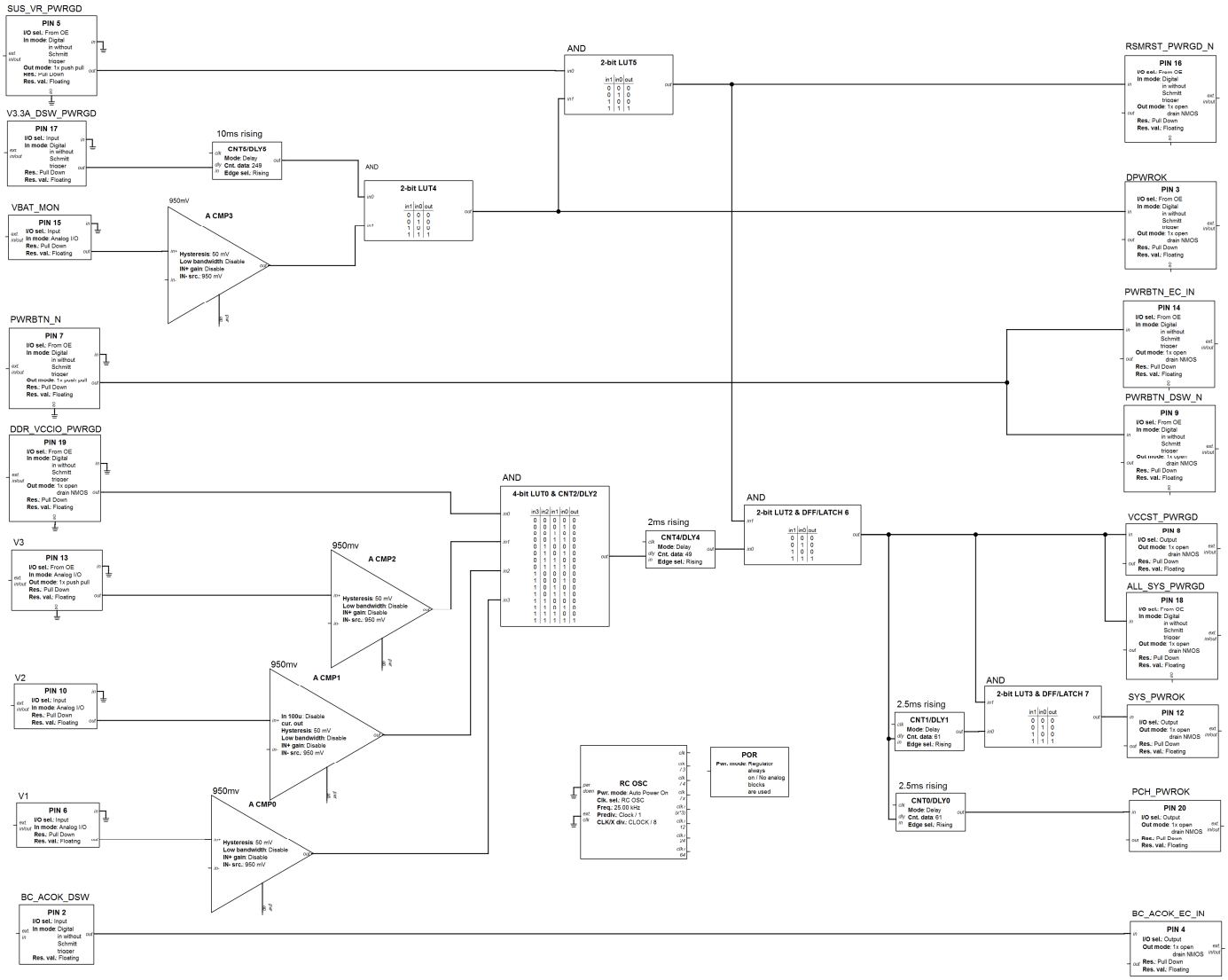
Output Summary

- 9 Outputs – Open Drain

Pin Configuration



Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	BC_ACOK_DSW	Input	Digital in without Schmitt trigger
3	DPWROK	Output	Open Drain
4	BC_ACOK_EC_IN	Output	Open Drain
5	SUS_VR_PWRGD	Input	Digital in without Schmitt trigger
6	V1	Input	Analog Input
7	PWRBTN_N	Input	Digital in without Schmitt trigger
8	VCCST_PWRGD	Output	Open Drain
9	PWRBTN_DSW_N	Output	Open Drain
10	V2	Input	Analog Input
11	GND	GND	Ground
12	SYS_PWROK	Output	Open Drain
13	V3	Input	Analog input
14	PWRBTN_EC_IN	Output	Open Drain
15	VBAT_MON	Input	Analog input
16	RSMRST_PWRGD_N	Output	Open Drain
17	V3.3A_DSW_PWRGD	Input	Digital in without Schmitt trigger
18	ALL_SYS_PWRGD	Output	Open Drain
19	DDR_VCCIO_PWRGD	Input	Digital in without Schmitt trigger
20	PCH_PWROK	Output	Open Drain

Ordering Information

Part Number	Package Type
SLG7NT4192V	V=TQFN-20
SLG7NT4192VTR	TQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C

Electrical Characteristics

(@ 25°C, unless otherwise stated)

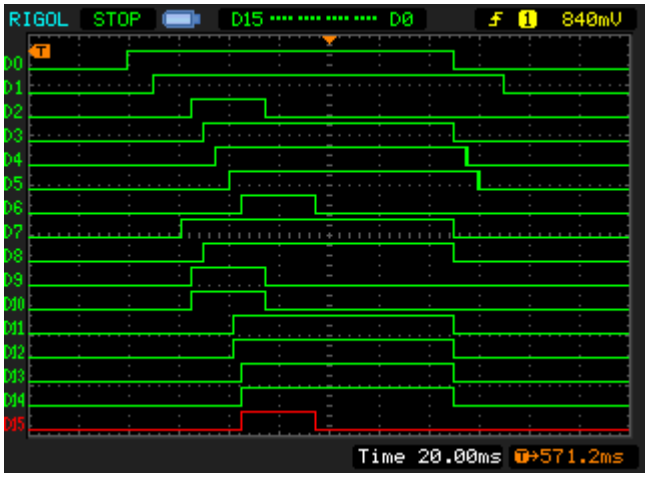
Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.135	3.3	3.465	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	85	--	µA
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.8	--	--	--
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.3	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN} =3.3V	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN} =0V	-1.0	--	1.0	µA
V_{OL}	LOW-Level Output Voltage	Open Drain, I_{OL} = 3 mA, 1X Driver	--	0.080	0.15	V
I_{OL}	LOW-Level Output Current	Open Drain, V_{OL} = 0.4 V, 1X Driver	7.3	12	--	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
V_{ACMP0}	Analog Comparator Reference Voltage	Including ACMP0 voltage reference	T.B.D.	950	T.B.D.	mV
V_{ACMP1}	Analog Comparator Reference Voltage	Including ACMP1 voltage reference	T.B.D.	950	T.B.D.	mV
V_{ACMP2}	Analog Comparator Reference Voltage	Including ACMP2 voltage reference	T.B.D.	950	T.B.D.	mV
V_{ACMP3}	Analog Comparator Reference Voltage	Including ACMP3 voltage reference	T.B.D.	950	T.B.D.	mV
V_{HYST}	Analog Comparator Hysteresis Voltage	ACMP0, ACMP1, ACMP2, ACMP3	T.B.D.	50	T.B.D.	mV
V_{OFFSET}	Analog Comparator Offset Voltage	ACMP0, ACMP1, ACMP2, ACMP3	--	±5	--	mV
T_{DLY0}	Delay0 Time		T.B.D.	2.5	T.B.D.	ms

T_{DLY1}	Delay1 Time		T.B.D.	2.5	T.B.D.	ms
T_{DLY4}	Delay4 Time		T.B.D.	2	T.B.D.	ms
T_{DLY5}	Delay5 Time		T.B.D.	10	T.B.D.	ms
T_{SU}	Start up Time		--	T.B.D.	--	ms

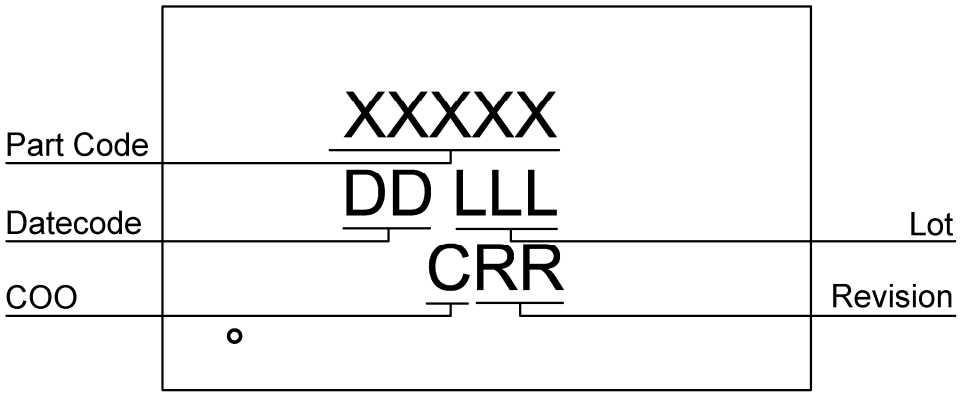
SLG7NT4192 Functionality Waveforms

Inputs:
D0 – Pin #15 (VBAT_MON)
D1 – Pin #17 (V3.3A_DSW_PWRGD)
D2 – Pin #7 (PWRBTN_N)
D3 – Pin #6 (V1)
D4 – Pin #10 (V2)
D5 – Pin #13 (V3)
D6 – Pin #2 (BC_ACOK_DSW)
Outputs:
D7 – Pin #3 (DPWROK) with external 5kΩ pull-up resistor
D8 – Pin #16 (RSMRST_PWRGD_N) with external 5kΩ pull-up resistor
D9 – Pin #14 (PWRBTN_EC_IN) with external 5kΩ pull-up resistor
D10 – Pin #9 (PWRBTN_DSW_N) with external 5kΩ pull-up resistor
D11 – Pin #8 (VCCST_PWRGD) with external 5kΩ pull-up resistor
D12 – Pin #18 (ALL_SYS_PWRGD) with external 5kΩ pull-up resistor
D13 – Pin #12 (SYS_PWROK) with external 5kΩ pull-up resistor
D14 – Pin #20 (PCH_PWROK) with external 5kΩ pull-up resistor
D15 – Pin #4 (BC_ACOK_EC_IN) with external 5kΩ pull-up resistor

1. Chip functionality (Pin5 (SUS_VR_PWRGD), Pin19 (DDR_VCCIO_PWRGD) are always HIGH)



Package Top Marking

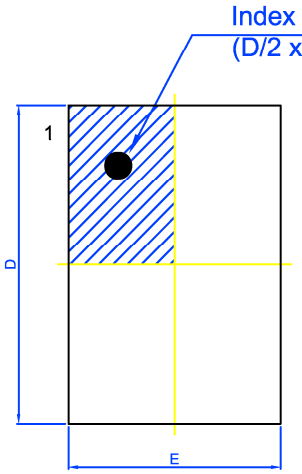


XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

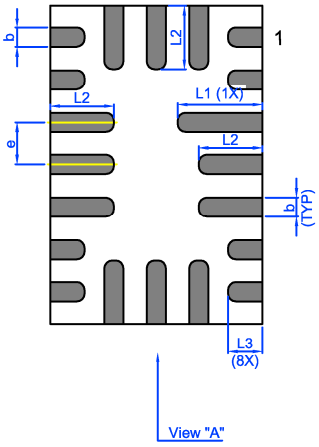
Datasheet Revision	Programming Code Number	Part Code	Revision	Date
0.11	02			05/27/2013

Package Drawing and Dimensions

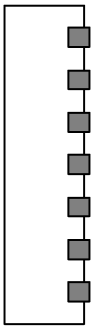
20 Lead TQFN Package
JEDEC MO-220, Variation WCEE



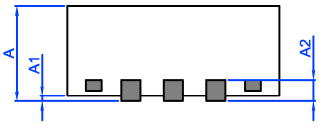
TOP VIEW



BOTTOM VIEW



SIDE VIEW



VIEW "A"

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.700	0.750	0.800	D	2.950	3.000	3.050
A1	0.000	-	0.050	E	1.950	2.000	2.050
A2	0.203 REF			L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.400 BSC			L3	0.275	0.325	0.375

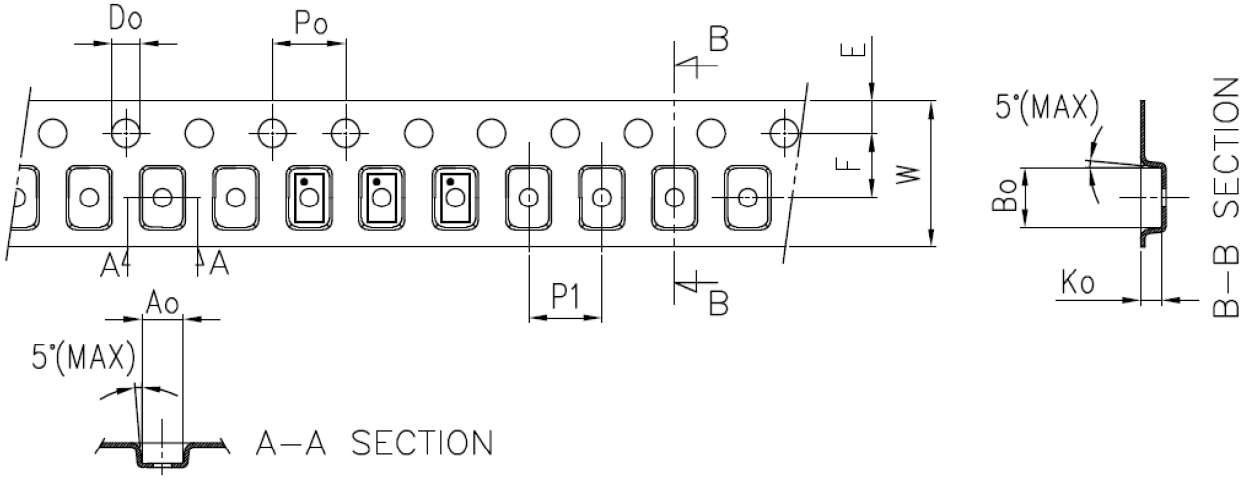
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TQFN 20L 2x3mm 0.4P Green	20	2x3x0.75	3000	3000	178/60	42	168	42	168	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TQFN 20L 2x3mm 0.4P Green	2.25	3.3	1.1	4	4	1.55	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 4.50 mm^3 (nominal). More information can be found at www.jedec.org.

Datasheet Revision History

Date	Version	Change
05/20/2013	0.1	New design
05/27/2013	0.11	Updated design

Silego Website & Support

Silego Technology Website

Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:

http://greenpak.silego.com/
http://greenpak2.silego.com/
http://greenfet.silego.com/
http://greenfet2.silego.com/
http://greenclk.silego.com/

Products are also available for purchase directly from Silego at the Silego Online Store at http://store.silego.com/.

Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send email requests to GreenPAK@silego.com

Users of Silego products can receive assistance through several channels:

Contact Your Local Sales Representative

Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

Contact Silego Directly

Silego can be contacted directly via e-mail at info@silego.com or user submission form, located at the following URL: http://support.silego.com/

Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of worldwide Silego Technology offices and representatives are all available at http://www.silego.com/

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